LISTING OF CLAIMS

1. (withdrawn) A method of forming a semiconductor device with increased latch-up robustness, the method comprising:

providing a p-type semiconductor substrate;

locating within said substrate an I/O pad having no direct connection to n-diffusions;

forming within said substrate an n-well;

forming within said n-well a silicide blocked p-type field effect transistor having a snapback voltage that is less than the breakdown voltage of the gate oxide of said transistor.

2. (currently amended) An ESD device comprising:

a silicide blocked p-type field effect transistor having a source, drain, gate, and gate oxide, said transistor further having a snapback voltage that is less than the breakdown voltage of said gate oxide and

wherein said gate is positioned between a p-diffusion of said source and a p-diffusion of said drain,

an n-diffusion is directly connected to said gate and said p-diffusion of said source and the n-diffusion is spaced apart from said p-diffusion of said source,

said transistor is coupled to an I/O pad that is connected to said p-diffusion of said drain and the I/O pad is located within a p-type semiconductor substrate, and

the I/O pad has no connection to n-diffusions of said transistor.

3. (original) The ESD device of claim 2 wherein said source is coupled to a voltage and said gate is coupled to said source and said drain is coupled said I/O pad.

4. (original) The ESD device of claim 2 further having a body terminal.

5. (original) The ESD device of claim 4 wherein said body terminal is coupled to said source.

6. (original) The ESD device of claim 2 wherein said snapback voltage is at most 5 volts.

7. (previously presented) The ESD device of claim 2 wherein a p-type resistor is coupled to said transistor and coupled to said I/O pad.

8. (original) The ESD device of claim 7 wherein said resistor is formed of p-type polysilicon.

9. (original) The ESD device of claim 7 wherein said resistor is a diffusion resistor.

10. (previously presented) The ESD device of claim 7 wherein said p-type resistor is located between a p-diffusion of said drain of said transistor and said I/O pad so that a first voltage appearing at said I/O pad is of a different magnitude than a second voltage appearing at said transistor, said first and second voltages differing by a value proportional to the resistance of said p-type resistor.

11. (currently amended) A latch-up robust integrated circuit comprising:

one or more I/O cells each having one or more I/O pads, wherein no n-diffusions are directly connected to the one or more I/O pads, and

wherein each of said one or more I/O pads is coupled to an associated and distinct one or more silicide blocked p-type field effect transistors having a source, drain, gate, and gate oxide, said transistor further having a snapback voltage that is less than the breakdown voltage of said gate oxide, and

wherein said gate is positioned between a p-diffusion of said source and a p-diffusion of said drain,

an n-diffusion is directly connected to said gate and said p-diffusion of said source and the n-diffusion is spaced apart from said p-diffusion of said source,

said transistor is coupled to an I/O pad that is connected to said p-diffusion of said drain and the I/O pad is located within a p-type semiconductor substrate, and

the I/O pad has no connection to n-diffusions of said transistor.

12. (original) The latch-up robust integrated circuit of claim 11 wherein each of said one or more I/O pads is coupled said drain of said associated and distinct one or more transistors and said source of said transistors is coupled to a voltage and said gate is coupled to said source.

13. (original) The latch-up robust integrated circuit of claim 12 wherein each of said transistors has a body terminal.

14. (original) The latch-up robust integrated circuit of claim 13 wherein said body terminal of each of said transistors is coupled to said source.

15. (original) The latch-up robust integrated circuit of claim 11 wherein said snapback voltage of each of said transistors is at most 5 volts.

16. (original) The latch-up robust integrated circuit of claim 11 wherein one or more p-type resistors is coupled to one or more of each of said one or more I/O pads.

17. (original) The latch-up robust integrated circuit of claim 16 wherein each of said one or more p-type resistors is formed of p-type polysilicon.

18. (original) The latch-up robust integrated circuit of claim 16 wherein each of said one or more p-type resistors is a diffusion resistor.

19. (previously presented) The latch-up robust integrated circuit of claim 16 wherein at least one of said one or more p-type resistors is located between the pad and a p-diffusion of said drain of an associated transistor of each of said I/O pads so that a first voltage appearing at any of said I/O pads is of a different magnitude than a second voltage appearing at the associated transistor, said first and second voltages differing by a value proportional to the resistance of the p-type resistor.